

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S64	5345	((Clock\$3 "clk" "ck" delay buffer driver) with (allocat\$4 distribut\$3 assign\$5 allot\$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic))) ((net adj list \$3) netlist\$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 11:48
S63	2880592	(schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 11:48
S65	2411	@ad< "20040331" And ((Clock\$3 "clk" "ck" delay buffer driver) with (allocat\$4 distribut\$3 assign\$5 allot\$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic))) ((net adj list \$3) netlist\$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 11:50
S66	80	@ad< "20040331" And ((Clock\$3 "clk" "ck" delay buffer driver) with (allocat\$4 distribut\$3 assign\$5 allot\$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic))) ((net adj list \$3) netlist\$3))) And ((verif\$7 check\$3 validat \$3) with (layout)) And	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 11:56

		((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration) with (skew\$3 delay))				
S67	75	@ad< "20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (allocat\$4 distribut\$3 assign\$5 allot\$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic")) module core) near2 (diagram drawing schematic))) ((net adj list \$3) netlist\$3))) And ((verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration) with (skew\$3 delay))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 11:57
S68	263	@ad< "20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic")) module core) near2 (diagram drawing schematic representation))) rtl synthesi\$5 translat\$3 ((net adj list\$3) netlist \$3))) And ((optim\$7 verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 12:13

		remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) with (skew \$3 delay Clock\$3 "clk" "ck" tree))				
S69	69	@ad< "20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic")) module core) near2 (diagram drawing schematic representation))) rtl synthesi\$5 translat\$3 ((net adj list\$3) netlist \$3))) And ((optim\$7 verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (skew\$3)) And ((add\$3 additional insert\$3 correct \$3 optim\$7 resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (delay buffer driver))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 12:22

S70	69	@ad<"20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic representation))) rtl synthesi\$7 translat\$3 ((net adj list\$3) netlist \$3))) And ((optim\$7 verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (skew\$3)) And ((add\$3 additional insert\$3 correct \$3 optim\$7 resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (delay buffer driver))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 12:23
S71	46	@ad<"20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic representation))) rtl synthesi\$7 hdl translat\$3 ((net adj list\$3) netlist \$3))) And ((optim\$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 12:37

		verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (skew\$3)) And ((add\$3 additional insert\$3 correct \$3 optim\$7 resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (delay buffer driver)) And (rtl (net adj list\$3) hdl netlist\$3)				
S72	46	@ad< "20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same ((schematic ((circuit "ic" cell gate instance wiring electrical component macro (logic near (user chip circuit "ic"))) module core) near2 (diagram drawing schematic representation))) rtl synthesi\$7 hdl translat\$3 ((net adj list\$3) netlist \$3))) And ((optim\$7 verif\$7 check\$3 validat \$3) with (layout)) And ((correct\$3 optim\$7 resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend \$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat \$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (skew\$3)) And ((add\$3 additional insert\$3 correct \$3 optim\$7 resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/08 12:44

	redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3) near6 (delay buffer driver)) And (rtl (net adj list\$3) hdl netlist\$3) and layout			
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